28.1 A Dual-Line Optical Transient Sensor with On-Chip Precision Time-Stamp Generation

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Conventional clocked line sensors generate large amounts of data when employed in high-speed short-latency machine vision applications because they read out data of all pixels at a fixed rate. For various problems such as measurement tasks, shape detection, object orientation extraction etc., a substantial fraction of the image data produced does not provide any information necessary to accomplish the function or to increase reliability or precision. One way to suppress image data redundancy is to use a self-timed data-driven sensor architecture.

The optical line sensor presented here combines an asynchronous pixel circuit with on-chip precision time-stamping and a synchronous bus arbiter. The temporal resolution of this new sensor is 100ns (compared to line rates on the order of 100kHz for the fastest clocked line sensors [1-4]) and is beneficial for various high-speed machine vision applications that do not rely on conventional image data. The output data volume depends on the dynamic contents of the scene and is typically orders of magnitude lower than equivalent data output produced by clocked line sensors in this type of applications.

Each pixel operates autonomously and responds with low latency to relative illumination changes by generating asynchronous events [5]. Pixels that are not stimulated do not produce outputs. The circuit combines an active continuous-time logarithmic photo-sensor with a self-timed differentiating switched-capacitor amplifier, threshold comparators and handshake logic. It generates two types of events, which represent a fractional increase or decrease in intensity that exceeds a tunable threshold. Combined with the pixel address, these events are referred to as 'address-events' (AE) [6]. The pixel is able to detect contrast changes of a few percent over a dynamic range of >120dB. The wide dynamic range arises from the logarithmic compression in the front-end photoreceptor circuit and the local (pixel intrinsic) event-based differentiation operation [5]. The 28T3C pixels measure 15μm×165μm in a standard 0.35μm CMOS process and are arranged in a 2×256 dual-line configuration with 15μm pixel pitch and 250μm line separation.

Time-stamps are traditionally assigned to asynchronous address-event data by a post-processor after arbitration of a shared communication channel, e.g. [6]. Depending on data rate and arbitration strategy, a non-deterministic variable latency affects the timing precision of the data [7-8]. The architecture presented here performs the time-stamp assignment at the pixel level. Time-stamps are combined with the corresponding address events to compose a synchronous stream of data packets. Events occurring during the same time-stamp period are interpreted as concurrent and are arbitrated in the order of their addresses. Pixel addresses and time-stamps are read out via a 3-stage pipelined synchronous bus arbiter. A single set of output data from the sensor is referred to as a 'timed address-event' (TAE).

A block diagram of the chip is shown in Fig. 28.1.1. Pixels signal positive (ON) and negative (OFF) illumination changes on separate terminals (R_x). The input stage EIF of the pixel arbiter (Fig. 28.1.2) stores events occurring for one time-stamp period; subsequently they are transferred to a bank of event-FIFO buffers (EFIFO). The EFIFOs handle event rate peaks while keeping the time-stamp period constant, even if the event peak-rate is higher than the maximum sustainable rate, as determined by the clock frequency. If all of the EFIFOs are full, the time-stamp period is enlarged temporarily to allow all stored data to be read out and to avoid data loss. Multiple events from one pixel occurring during the prolonged time-stamp period will be suppressed.

The arbiter consists of three functionally similar hierarchical stages: the event arbiter EARB, the address-event arbiter AEARB (Fig. 28.1.2), and the line arbiter (Fig. 28.1.1). The arbiter control block starts the arbitration process upon arrival of data in the EFIFOs by asserting the *event_fetch* signal. Address events are generated in the EARB units by assigning the address according to the selected input to the current time-stamp, while a look-ahead circuit simultaneously determines the next active input and clears the event from the event buffer. The AEARB unit selects the next EARB unit after the current EARB has processed all available events, which it signals by AE_p_avail. The line arbiter arbitrates the two pixel arbiter blocks in a similar way. All three arbiter stages work in a pipelined manner and use the same look-ahead strategy.

The time-stamp value and corresponding address events are transferred sequentially over a 16b-wide data bus. A counter wrap-around bit is included in the TAE data, enabling the post-processor to perform a time-stamp value expansion. The chip has been verified to run at a clock frequency of 40MHz, leading to a minimum time-stamp resolution of 100ns and a maximum transfer rate of 320Mb/s.

Various machine vision applications call for high-resolution measurement of edge angles of fast moving objects [9]. Fig. 28.1.3 shows TAEs from one sensor line in response to the stimulus depicted in the inset. The stimulus pattern consists of a series of bars at orientations varying from 90 to 175 degrees in 5 degree steps. The bars were moved at velocities up to 23m/s at a distance of 15cm from the sensor (f/1.6, 8mm lens). In this application example, the sensor delivers data at a rate of 3.6Mb/s, which is about 10 times less than a comparable line-scan sensor, e.g. [2], for equal temporal resolution and information content.

The time-stamps are converted to isogonal spatial information by means of an object speed measurement based on correlation of the data from the two pixel lines. Fig. 28.1.4 shows projected Hough transform [10] angle histograms of the leading edges of each stimulus bar for one pass of the pattern at 3.5m/s and 23m/s, recorded at ~500lx scene illumination (typical office light). Stimulus and setup imperfections, lens distortions, time-stamp quantization, pixel latency jitter, etc. all cause shifts and non-zero full-width-at-half-maximum (FWHM) of the angle histogram peaks. No degradation of performance has been observed up to the highest available (to us) stimulus speed of about 23m/s, e.g. FWHM of the angle histograms remain practically constant. The preliminary results shown in Fig. 28.1.5 indicate that the sensor is able to resolve angle differences of 0.25 degrees or less. Limits to the sensor operation regarding object speed and angle resolution have not yet been determined. The sensor was fabricated in a 0.35μm standard CMOS process and consumes 250mW at 40MHz. The specifications are summarized in Fig. 28.1.6 and Fig. 28.1.7 shows a micrograph of the chip with dimensions 3.6×5.2mm^2.

The dual-line configuration provides additional functionality, such as measurement of trajectory angles by correlating TAE streams from the two parallel pixel lines. The high dynamic range makes this sensor suitable for use under difficult or variable lighting conditions as occur in outdoor applications. The sparse data delivered by the sensor require low computational effort in the subsequent processing stages and allow for compact and low-cost embedded systems.

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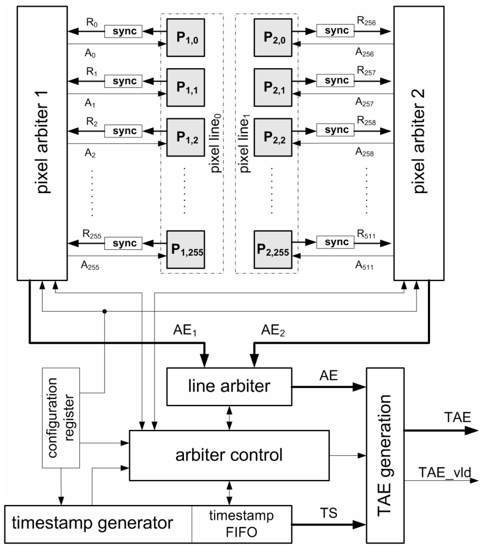

Figure 28.1.1: Block diagram of the dual-line sensor.

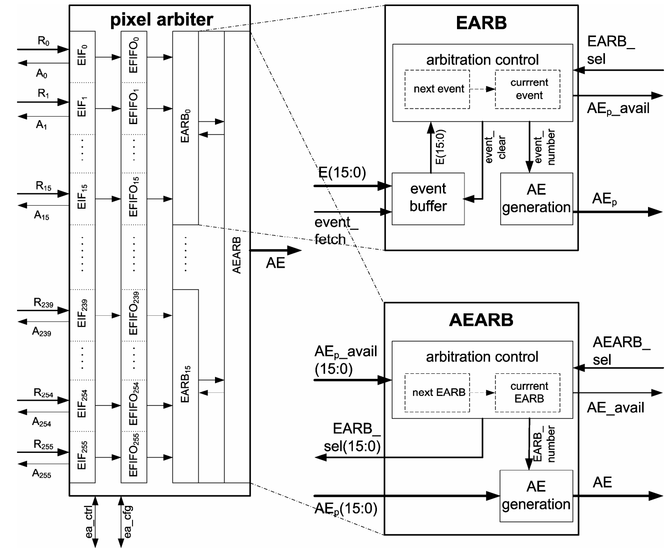

Figure 28.1.2: Block diagram of the pixel arbiter.

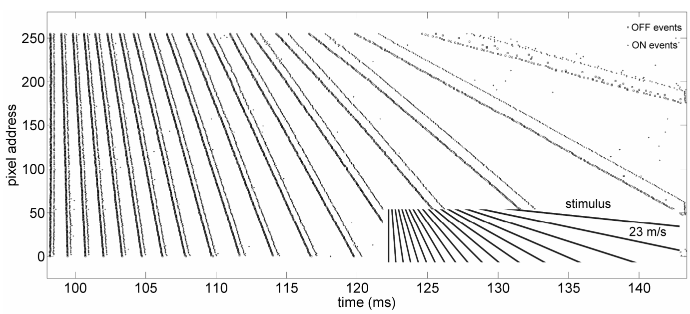

Figure 28.1.3: Sensor output TAEs of one pixel line (x-axis time is not scaled for isogonal spatial coordinates).

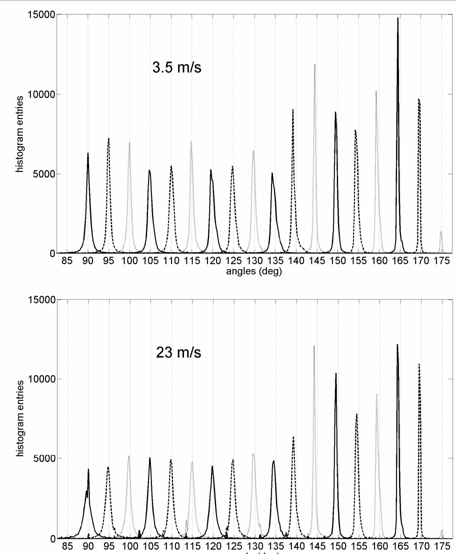

Figure 28.1.4: Angle histograms for two stimulus speeds.

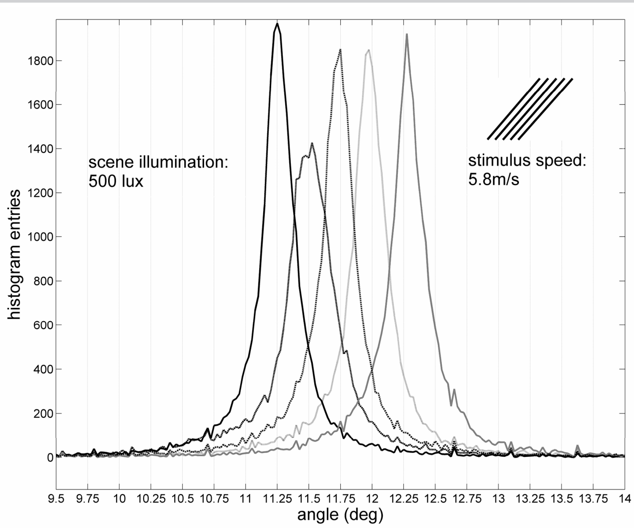

Figure 28.1.5: Angle histograms of edges with orientations varying by 0.25 degrees (inset shows the stimulus pattern).

Fabrication process	4-Metal 2-Poly 0.35µm standard CMOS
Die size	3.6×5.2mm^2
Sensor configuration	2×256, 15µm pixel pitch, 250µm line separation
Pixel size	15µm×165µm
Pixel complexity	28 transistors, 3 capacitors
Fill factor	80%
Dynamic range	> 120dB
Minimum scene illumination (f/1.4)	~ 0.1lx
Operating frequency	40MHz
Time-stamp period	$2^2/f_{clk} - 2^{16}/f_{clk}$ (steps of 4)
Max. output bit rate	320 Mbit per second
Max. output event rate	$20 \cdot 10^6$ events per second
Power consumption	max. 250mW @ 3.3V
Interface	TAE protocol, 16-bit parallel AE: ID, polarity, line address (13:12), pixel address (11:0) Time-stamp: ID, wrap-around, overflow, time-stamp (12:0)

Figure 28.1.6: Summary of specifications.

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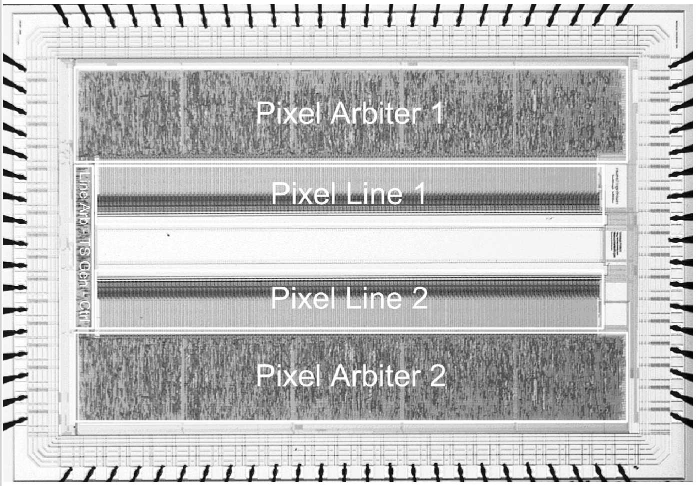

Figure 28.1.7: Chip micrograph.

